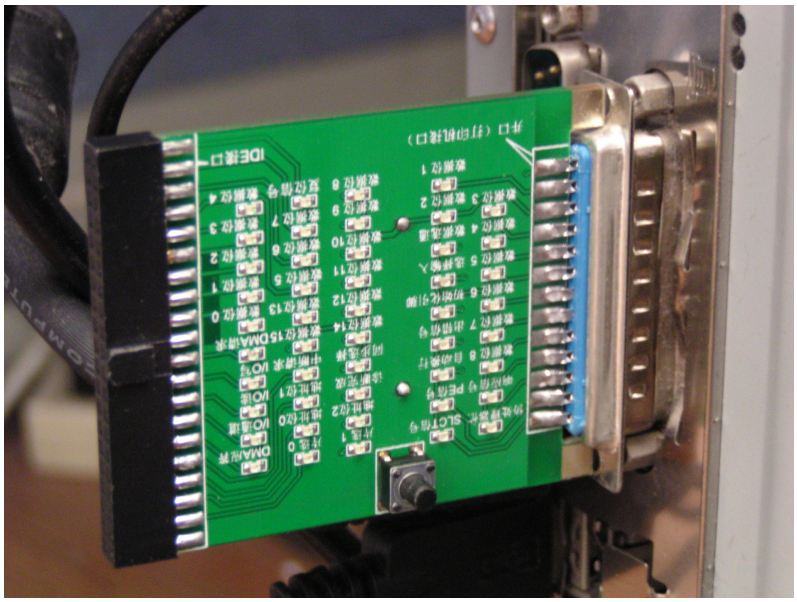
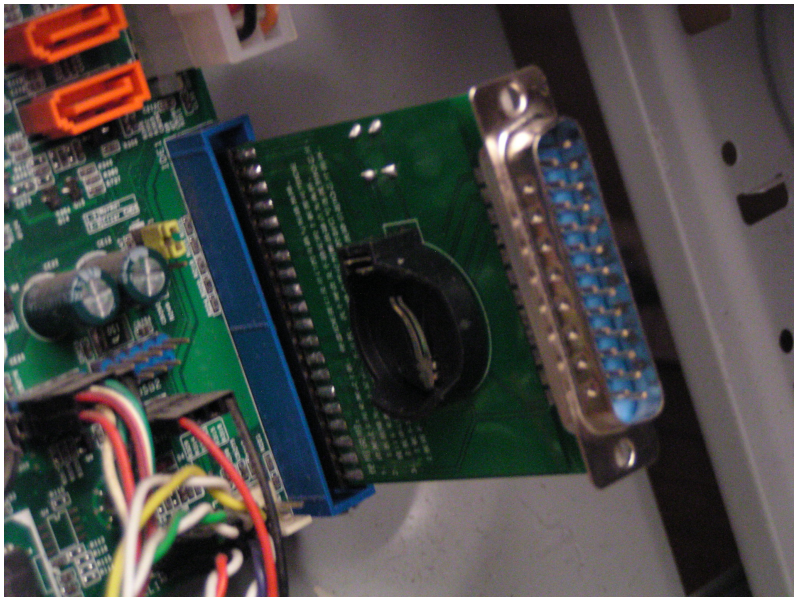
LPT & IDE Tester

The LPT & IDE tester is for testing open circuit or short circuit occurs in hard drive IDE port / parallel port on the mainboard. Mainboard error always shows as “no display”, “fail to bootup”, “fail to find the hard drive” or “Mainrboard working unstable”. All these problems can be tested by LPT & IDE tester. As long as open circuit or short circuit can be found out, the error would be south bridge.

The following two photos show the connection of the tester.



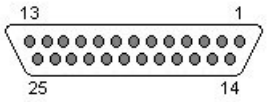


When plug the tester to the PC and reboot the PC, the following screen will show if the PC work well.
Remark: The CR 2032 battery must be inserted in battery slot before using it.

How to determine the port working well?
*** It doesn't need to power up the PC, just plug into right slot and press the switch. Each of LEDs represent a specify address bus. If ALL of LEDs of IDE/LPT port are turned on, then the port works well. Otherwise, please check with the diagram shown as follows which can determine the failure address

Diagram for LPT port:

Parallel (PC)



(At the PC)

25 PIN D-SUB FEMALE at the PC.

Pin	Name	Dir	Description
1	/STROBE	→	Strobe
2	D0	→	Data Bit 0
3	D1	→	Data Bit 1
4	D2	→	Data Bit 2
5	D3	→	Data Bit 3
6	D4	→	Data Bit 4
7	D5	→	Data Bit 5
8	D6	→	Data Bit 6
9	D7	→	Data Bit 7
10	/ACK	←	Acknowledge
11	BUSY	←	Busy
12	PE	←	Paper End
13	SEL	←	Select
14	/AUTOFD	→	Autofeed
15	/ERROR	←	Error
16	/INIT	→	Initialize
17	/SELIN	→	Select In
18	GND	—	Signal Ground
19	GND	—	Signal Ground
20	GND	—	Signal Ground
21	GND	—	Signal Ground
22	GND	—	Signal Ground
23	GND	—	Signal Ground
24	GND	—	Signal Ground
25	GND	—	Signal Ground

Note: Direction is Computer relative Device.

IDE Signal List:

Pin	Signal Name	Signal Description	Signal Direction	ISA Main Cable Signal
1	RESET	RESET	I	RESET (polarity opposite)
3	DD7	DATA ADDRESS 7	I/O	D7
5	DD6	DATA ADDRESS 6	I/O	D6
7	DD5	DATA ADDRESS 5	I/O	D5
9	DD4	DATA ADDRESS 4	I/O	D4
11	DD3	DATA ADDRESS 3	I/O	D3
13	DD2	DATA ADDRESS 2	I/O	D2
15	DD1	DATA ADDRESS 1	I/O	D1
17	DD0	DATA ADDRESS 0	I/O	D1
19	GND	GND		GND
21	DMARQ	DMA REQUEST	O	DRQx
23	BIOW	I/O WRITE	I	IOW
25	DIOR	I/O READ	I	IOR
27	IORDY	I/O CHANNEL PREPARATION	O	IO CH RAY
29	DMACK	I/O RESPONSE	I	DACKx
31	INTRQ	BREAK OFF REQUEST	I	IRQ14
33	DA1	ADDRESS 1	I	A1
35	DA0	ADDRESS0	I	A0
37	CSO	SEGMENT 0	I	
39	DASP	CPU ACTIVATION	O	
2	GND	GND		GND
4	DD8	DATA ADDRESS 8	I/O	D8
6	DD9	DATA ADDRESS 9	I/O	D9
8	DD10	DATA ADDRESS 10	I/O	D10
10	DD11	DATA ADDRESS 11	I/O	D11
12	DD12	DATA ADDRESS 12	I/O	D12
14	DD13	DATA ADDRESS 13	I/O	D13
16	DD14	DATA ADDRESS 14	I/O	D14
18	DD15	DATA ADDRESS 15	I/O	D15
20	KEYPIN	FOR POSITION		X
22	GND	GND		GND
24	GND	GND		GND
26	GND	GND		GND
28	SPYSNC:CSEL	SYNCHRONOUS OR CABLE		

		CHOOSING		
30	GND	GND		GND
32	IOCS16	16DIGIT I/O	O	I/OCS16
34	PDIAG	TESTING COMPLETE	O	
36	DA2	ADDRESS 2	I	A2
38	CS1	SEGMENT 1	I	
40	GND	GND		GND

~ END ~